**Simulation Assignment #2**

**Additional Verilog Construct Usage, Testbench Development Techniques, and Simulation**

**Assignment**

(a)   Write a parameterized Verilog module named *ones\_count.v* which has an input port declarations for the bus named *in\_vec*, and an output port declaration for the bus named *count*. Assume that the number of bits in *in\_vec* is given by the the module’s Verilog *parameter*, N, which is assigned a default value of 16. Also assume that the size of *count* is 16 bits and is treated as an unsigned data type. The module should be combinational in nature employing no clocking signal. It should be encoded in a behavioral manner that incorporates an *always* secton that contains a single *for* loop.

(b) Write a Verilog testbench, named *ones\_cout\_tb.v* that will provide a new stimulus to the *in\_vec* input of the *ones\_count* module every 10 ns for the 16 distinct *in\_vec* values that are read from the file *in\_vec\_input.txt* which is a 16 line text file where the data is encoded in hexadecimal format. The Ver­ilog testbench should also record the resulting count value that is produces by the ones\_count module for each *in\_vec* input and place it in the text output file named *count\_output*.txt. The *count* data in this text file should be in decimal format with each *count* value being shown on a separate line.

(c)   Simulate this design using ModelSIMtm using the testbench developed in Part (b). Before doing this set the value of N to 32 in your testbench (overriding its default of 16) when you instantiate the *ones\_count* module. Also enter 16 stimulus data points in the *in\_vec\_input.txt* files in hexadecimal format. Chose values of test vectors that should provide a wide range of *count* values in a correctly operating design. Verify the correctness of the results in the *count\_output.txt* file.

(d)  Create a modified version of the *ones\_count.v* count, named *ones\_count\_task.v* that utilizes a task con­struct and a call to the task. The task call should have the following format: ***task\_name(A,B)*** where ***A*** is the input and ***B*** is the output. Verify the correctness of the design through simulation using the testbench developed in Part (b) and the same input stimulus in the *in\_vec\_input.txt* file.

(e)   Create another modified version of the *ones\_count.v*, named *ones\_count\_function.v* that utilizes a func­tion construct and a call to that function within the *ones\_count\_function.v* module. Verify the correctness of the design through simulation using the testbench developed in Part (b) and the same input stimulus in the *in\_vec\_input.txt* file.

       Submissions of this assignment should be made on Canvas. It should include the fully commented the *ones\_count.v*, *ones\_count\_tb.v*, *ones\_count\_task.v*, *ones\_count\_function.v* and the resulting *count\_output.txt* files from part c, d, and e.